CLAIMS

WHAT IS CLAIMED:

1. A method, comprising:

identifying a relationship between a capacitive coupling of a conductor and a doped region formed in a semiconducting substrate under said conductor based upon an overlap between said conductor and said doped region;

forming a second doped region under a second conductor; and

assessing a lateral dimension of an overlap of said second doped region with said second conductor based upon said identified relationship.

2. The method of claim 1, wherein said identified relationship is a linear relationship.

3. The method of claim 1, wherein said identified relationship is a non-linear relationship.

4. The method of claim 1, wherein identifying said relationship includes:

determining a first capacitive coupling of a reference dopant profile formed in said doped region to said conductor laterally offset from said reference dopant profile by a first dielectric region having a first offset thickness; and

determining a second capacitive coupling of said reference dopant profile formed in a third doped region to a third conductor laterally offset from said reference dopant profile by a second dielectric region having a second offset thickness.

5. The method of claim 4, further comprising:

determining a capacitive coupling of a test dopant profile formed in said second doped region to said second conductor laterally offset from said second doped region by a third dielectric region having a predefined offset thickness; and

assessing a lateral distribution of said test dopant profile on the basis of said first and second capacitive couplings and said first, second and predefined offset thicknesses.

6. The method of claim 5, wherein said reference dopant profile and said test dopant profile, said conductor and said second and third conductors and said doped region and said second and third doped regions are portions of a first, a second and a third transistor structure, respectively.

7. The method of claim 6, wherein the dimensions and materials of said first, second and third transistor structures are substantially identical.

8. The method of claim 5, further comprising establishing a mathematical relationship between said first and second capacitive couplings and said first and second offset thicknesses, respectively.

9. The method of claim 8, further comprising determining a change of capacitive coupling for a variation of offset thickness for said reference dopant profile.

10. The method of claim 5, wherein said predefined offset thickness is substantially the same as one of said first and the second offset thicknesses.

11. The method of claim 5, further comprising determining a difference of a lateral extension of said reference dopant profile and said test dopant profile.

12. A method, comprising:

determining a first capacitive coupling of a reference dopant profile formed in a first semiconductor region to a first conductive region laterally offset from said reference dopant profile by a first dielectric region having a first offset thickness;

determining a second capacitive coupling of said reference dopant profile formed in a second semiconductor region to a second conductive region laterally offset from said reference dopant profile by a second dielectric region having a second offset thickness;

determining a capacitive coupling of a test dopant profile formed in a third semiconductor region to a third conductive region laterally offset from said third semiconductor region by a third dielectric region having a predefined offset thickness; and

assessing a lateral distribution of said test dopant profile on the basis of said first and second capacitive couplings and said first, second and predefined offset thicknesses.

13. The method of claim 12, wherein said reference dopant profile and said test dopant profile, said first, second and third conductive regions and said first, second and third dielectric regions are portions of a first, a second and a third transistor structure, respectively.

14. The method of claim 13, wherein the dimensions and materials of said first, second and third transistor structures are substantially identical.

15. The method of claim 12, further comprising establishing a mathematical relationship between said first and second capacitive couplings and said first and second offset thicknesses, respectively.

16. The method of claim 15, further comprising determining a change of capacitive coupling for a variation of offset thickness for said reference dopant profile.

17. The method of claim 12, wherein said predefined offset thickness is substantially the same as one of said first and the second offset thicknesses.

18. The method of claim 12, further comprising determining a difference of a lateral extension of said reference dopant profile and said test dopant profile.

19. The method of claim 18, further comprising performing a simulation for a process of forming said reference dopant profile and said test dopant profile; and comparing a result of said simulation with said difference.

20. The method of claim 19, further comprising simulating said first, second and third capacitive couplings by small signal simulation and obtaining a theoretical value of said difference of the lateral extension on the basis of said process simulation and said small signal simulation result.

21. The method of claim 12, further comprising simulating a two-dimensional formation process for forming said reference dopant profile and said test dopant profile and adapting said two-dimensional process simulation on the basis of said lateral distribution.

22. A method of assessing an implanted dopant profile, the method comprising:

forming a first gate electrode structure with a first sidewall spacer having a first width;

forming a second gate electrode structure with a second sidewall spacer having a second width;

forming a dopant profile adjacent to said first and second gate structures with substantially the same process conditions and using said first and second sidewall spacers as an implantation mask, each dopant profile acting as source and drain of a first transistor and a second transistor; and

determining an overlap capacitance of said first and second transistors to establish a dependence of overlap capacitance variation with spacer width variation for said dopant profile.

23. The method of claim 22, wherein said first and second gate structures are substantially identical.

24. The method of claim 22, further comprising forming a third transistor having a gate electrode structure with a predefined sidewall spacer width with a test dopant profile.

25. The method of claim 24, further comprising determining an overlap capacitance of said third transistor and estimating a lateral extension of said test dopant profile on the basis of said dependence.

26. The method of claim 24, wherein said predefined sidewall spacer width of said third transistor substantially corresponds to one of said first and second spacer widths.

27. The method of claim 22, further comprising:

forming at least one more transistor having said dopant profile and having a sidewall spacer width other than said first and second widths; and

determining an overlap capacitance of said at least one more transistor.

28. The method of claim 27, wherein establishing said dependence comprises obtaining a mathematical expression based on the overlap capacitances of said first, second and the at least one more transistors.

29. The method of claim 22, further comprising performing a simulation for a process of forming said dopant profile and comparing a result of said simulation with said dependence.

30. The method of claim 29, further comprising adapting said dependence in accordance with a result of said comparison.

31. The method of claim 22, further comprising simulating said overlap capacitances of said first and second transistors by small signal simulation and obtaining a theoreti-

cal value of a lateral extension of said profile on the basis of said process simulation and said small signal simulation result.

32. The method of claim 24, further comprising determining a difference in the lateral extension of said dopant profile and said test dopant profile by using said dependence and said predefined sidewall spacer width.

33. The method of claim 22, wherein said first and second transistors are formed on a common substrate.

34. The method of claim 22, wherein said first, second and third transistors are formed on a common substrate.

35. The method of claim 24, wherein at least one process parameter of a formation process in forming said test dopant profile is changed compared to a formation process of said dopant profile.

36. The method of claim 35, wherein said at least one process parameter relates to at least one of an implantation process and an annealing process.